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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,072	03/25/2004	Karl Pichler	NSL-030	3530

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EXAMINER	
LEE, GRANVILL D	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,072	PICHLER, KARL	
	Examiner	Art Unit	
	Granvill D. Lee Jr	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/24,3/25/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Pub. 2003/0189215) in view of Cok et al. (US Pub. 2004/0032220).

In regard to these claims (esp. clm. 1), Lee et al. teaches a method for manufacturing optoelectronic light emitting (LED) devices (Title), comprising the steps of, forming a layered structure having a plurality of layers (Fig. 12) including a bottom electrode layer (#128), a top electrode layer (#160), and one or more active layers (#126) between the top and bottom electrode layers; cutting through one or more of the layers of the layered structure to divide the layered structure into one or more separate device sections (Fig. 4). Lee et al. teaches that each section having a portion of the active layer disposed between portions of the top and bottom electrode layers (Fig. 4). Lee et al. further teaches an unpattern device followed by cutting at least to the substrate of the LED device (Fig. 4). But, Lee et al. fails in assembling two or more device

sections into a module; and electrically connecting the bottom electrode layer portion of one device section to the top electrode layer portion of another device section in serial fashion. Yet, Cok et al. discloses a LED device where the bottom electrode layer portion of one device section to the top electrode layer portion of another device section in serial fashion.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the LED device of Lee et al. in favor of the serial process of Cok et al. with the goal of producing individually series connected LED's which together are supplied by one source. Cok et al. sought a process where a multiplicity of spaced apart LED devices could be used in an area of illumination apparatus (Para. 34) and still have a low voltage source (Para. 37).

In view of claims 2-3, Lee et al. teaches a LED structure that includes cutting through a substrate layer and all the layers of the layered structure (Fig. 15).

In view of claims 4, Lee et al. also teaches all of the layers of the layered structure are unpatterned layers at the time of cutting (Fig. 4).

In view of claim 5, both Cok et al. and Lee et al. discloses protecting an edge of a device section against undesired electrical contact between two or more of the bottom electrode, top electrode and active layer portions (Cok-Para 119, Lee-Fig. 13 #162).

In regard to claim 6, Lee et al. further discloses protecting an edge of a device section includes the step of, before cutting through one or more of the layers of the layered structure, placing short-proofing material (#162) between adjacent layers of the layered structure proximate a location where the layered structure is to be cut (Para. 49).

In regard for claims 7-8, Lee et al. teaches that protecting an edge of a device section includes the step of passivating and insulating a side using oxygen for the device section (Para 47-48).

In regard for claim 9, Cok et al. discloses assembling two or more device sections into a module includes the step of laminating the two or more device sections side-by-side (Fig. 7b) between layers of laminating material (#48a).

In regard for claim 10, Lee et al. discloses before cutting through one or more of the layers of the layered structure to divide the layered structure into one or more device sections, patterning the top electrode layer and/or active layers to device the one or more device module sections (Para. 34-35).

In regard for claim 11, Lee et al. discloses further protecting an edge of a device section against undesired electrical contact between two or more of the bottom electrode, top electrode and active layer portions of the one or more device module sections (Figs. 14-15 #162).

In the method of claim 12, Lee et al. teaches protecting an edge of a device section includes the steps of, after patterning the top electrode layer (#128) and/or active layers, disposing an insulating material (Fig. 13 #162)

between the active layer portions of two or more adjacent device sections (Fig. 15).

In view of claim 13, Lee et al. discloses forming a layered structure includes covering the active layer (#126) and the insulating (buffer) material with an unpatterned top electrode layer (Fig. 4 #128) before cutting the layered structure to divide the layered structure into one or more device sections.

In view of claim 14, Lee et al. further teaches cutting the layered structure includes cutting the layered structure at locations corresponding to the insulating material (Fig. 15 #162).

In view of claim 15, Lee et al. further teaches electrically connecting the bottom electrode layer portion of one device section to the top electrode layer portion of another device section includes the steps of: exposing a portion of an upper surface of the bottom electrode layer portion of a first device section; and connecting an electrically conductive material between the top electrode layer portion of a second device section and the exposed portion of the upper surface of the bottom electrode layer in serial fashion (Fig. 7b).

In regard to claims 16-17, Cok et al. discloses photovoltaic cells (Fig. 2a) representing the organic light emitting device (OLED) (Para. 36).

Contact Information

Any inquiry concerning this communication or earlier communications for the examiner should be directed to Granvill Lee

whose telephone number is (571) 272-1897. The examiner can be normally reached on Monday thru Friday from 6:00 am to 2:30 pm.

If attempts to reach the examiner by telephone are not successful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Granvill Lee
Art Unit 2891

Gl
8/4/05

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